REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the non-final Office Action of May 18, 2004 (hereinafter "Office Action"). In response, Applicants have canceled Claims 21 – 24. Applicants submit, however, that the cited references fail to disclose or suggest, at least, all of the recitations of the pending independent claims; therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1 and 11 are Patentable

Independent Claims 1 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,078,978 to Suh (hereinafter "Suh") in view of U. S. Patent No. 6,701,446 to Tsern et al. (hereinafter "Tsern") and U. S. Patent No. 6,185,145 to Merritt (hereinafter "Merritt"). Independent Claim 1 is directed to a memory interface system and recites:

> at least one channel line that couples a memory to a memory controller, the at least one channel line being responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage.

Independent Claim 11 includes similar recitations. As illustrated in FIG. 1, for example, of the present Specification, a memory interface system is shown in which the terminal voltage VTER is independent of the memory supply voltage VDD1 and the memory controller supply voltage VDD2. The Office Action alleges that when the teachings of the Suh, Tsern, and Merritt references are combined, the result is that three independent power supplies are used: one for the controller, one for the line, and one for the memory itself. (Office Action, page 4).

Applicants respectfully disagree with this interpretation of the teachings of Suh, Tsern, and Merritt. Turning first to Suh, Applicants acknowledge that Suh describes a bus interface circuit shown in FIG. 1 in which a reference voltage Vref is generated based on a terminal voltage Vtt using an off-chip network of resistors R1 and R2 (Suh, col. 2, lines 1 – 20). Applicants submit, however, that Suh appears to be silent with regard to the voltage source used to power the receiver 13. Suh explains that the "environment of the transmission

line for the data signal is different than that of the transmission line for the reference voltage signal." (Suh, col. 4, lines 32 – 34). Thus, while Suh describes interface circuits in which the transmission line for the reference voltage signal is off-chip while a transmission line for a data signal is on-chip, Suh does not appear to describe what voltage is used to power the receiver 13. Thus, Suh contains no teaching or suggestion of making the voltage that drives the receiver 13 and the terminal voltage Vtt independent from one another.

Turning next to Tsern, this reference illustrates a memory system in FIG. 2A in which a terminal voltage Vterm is used to drive both data and control buses. Tsern, however, appears to contain no disclosure or suggestion with respect to what voltages are used to power the controller 12 and the memory blocks 16. Thus, Tsern contains no teaching or suggestion of making voltages that power the controller 12 and the memory blocks 16 independent of the terminal voltage Vterm that is used to drive the data and control buses.

Turning finally to Merritt, this reference discloses a system in FIG. 1 in which the voltage VCC2 used to power the logic section 200 is also used to drive the line carrying the data signal VIN. Thus, Merritt does not disclose a system in which the voltage used to drive the data line is independent of the logic section 200.

In view of the analysis above, Applicants respectfully submit that Suh, Tsern, and Merritt, either alone or in combination, do not disclose or suggest a channel line that is responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage as recited in Claims 1 and 11.

Accordingly, for at least the foregoing reasons, Applicants respectfully submits that independent Claims 1 and 11 are patentable over Suh in view of Tsern and Merritt and that Claims 2 – 10 and 12 - 20 are patentable at least per the patentability of independent Claims 1 and 11.

Dependent Claims 5, 9, 10, 15, 19, and 20 are Separately Patentable

Applicants respectfully submit that dependent Claims 5, 9, 10, 15, 19, and 20 are patentable over the cited references for at least the reasons set forth above with respect to Claims 1 and 11. Dependent Claims 5, 9, 10, 15, 19, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Suh in view of Tsern, Merritt, and U. S. Patent No. 5,450,365 to Adachi (hereinafter "Adachi").

Claims 5, 9, 15 and 19 recite a first and second level shifter circuits that couple first and second channel lines to first and second receivers/differential amplifier circuits. Applicants respectfully submit that Merritt discloses a system in which a level shifter (reference voltage generator 13) is used to couple a reference voltage line to a receiver (signal comparator 15), not a channel line that is responsive to a terminal voltage that is independent of both a memory supply voltage and a memory controller supply voltage. Moreover, Adachi fails to provide the missing teaching as this reference describes a control interface in which all signals between a memory card and a processing device are level shifted to account for the different operating voltages between the two components. Level shifting all voltages would be incompatible with the teachings of Merritt as the reference voltage generator 13 is used to generate a specific trip point for the signal comparator 15 (see Abstract). If all voltages were level shifted in concert then such trip point tuning would not be possible.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that dependent Claims 5 and 15 are separately patentable over Suh, Tsern, Merritt, and Adachi.

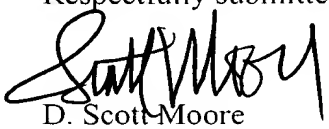
Claims 10 and 20 recite that the magnitude of the terminal voltage is greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively. As discussed above, Suh contains no disclosure with regard to the nature of the voltage used to power the receiver 13 and Tsern contains no disclosure with regard to the nature of the voltage(s) used to power the controller 12 and the memory blocks 16. Merritt, however, discloses a system in which a voltage VCC2 is used to power the logic section 200 and is also used to drive the line carrying the data signal VIN. Thus, in Merritt the voltage used to drive the line carrying the data signal VIN is not greater than the magnitude of the voltage used to power the logic section 200, but is instead the same voltage. Moreover, Adachi fails to provide the teachings missing from Suh, Tsern, and Merritt. Thus, none of the cited references disclose or suggest using a terminal voltage that has a magnitude greater than the magnitudes of the memory supply voltage and the controller supply voltage, respectively, as recited in Claims 10 and 20.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that dependent Claims 10 and 20 are separately patentable over Suh, Tsern, Merritt, and Adachi.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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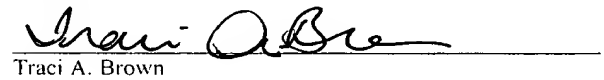

Traci A. Brown